REMARKS

Claims 1-36 were pending in the application. Claims 1, 6, 12, 21, and 30 have been amended. Accordingly, claims 1-36 are pending in the application.

INFORMATION DISCLOSURE STATEMENT

As noted above, under 37 CFR 1.98(d), submission of the IDS references is not believed necessary.

SPECIFICATION

Pursuant to the examiner's request, Applicant has updated the application status information on page 1 of the specification.

CLAIM REJECTIONS

35 U.S.C. § 103 REJECTIONS

In the present Office Action, claims 1-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,041,062 (hereinafter "Yamato"), in view of U.S. Patent 4,704,715 (hereinafter "Shibagaki"), in further view of U.S. Patent 6,055,242 (hereinafter "Doshi"), in further view of Applicant's admitted prior art. Applicant respectfully traverses these rejections and requests reconsideration in view of the following discussion.

Applicant submits that claim 1 recites features which are neither disclosed nor suggested by the cited art. In paragraph 6 of the present Office Action, the examiner states that Yamato discloses:

> "generating at least two low-speed data channels (col. 4, lines 38-54 and col. 5, lines 6-13), where multiplexing STM-0 into high-order STM signals indicates two or more low-speed channels, wherein the low-speed data channels in aggregate contain the recovered data and each low-speed channel is timed by a clock based on the reference clock (col. 5, lines 32-33 and col.7, lines 15-34); and multiplexing the low-speed symbol channels to produce an electrical high-speed channel for transmission in optical form across the communication system (Fig. 6; col. 7, lines 15-34; and col. 8, lines 15-23)."

However, claim 1, as amended, recites a method which includes:

> "receiving a tributary complying with a jitter tolerance;
> recovering data from the tributary;
> receiving a reference clock;
> converting the recovered data into at least two low-speed data channels, wherein the low-speed data channels in aggregate contain the recovered data and each low-speed data channel is timed by a clock based on the reference clock;
> modulating each low-speed data channel to generate a corresponding low-speed symbol
> channel; and
> frequency division multiplexing the low-speed symbol channels to produce an electrical high-speed channel for transmission in optical form across the communications system."

It is noted that the recited converting, modulating, and multiplexing in Claim 1 are related to one another and occur in a particular order with respect to one another. For example, recovered data is converted to at least two data channels, each of the resulting data channels are modulated to generate a corresponding symbol channel, and the resulting symbol channels are multiplexed. Applicant submits that while Yamato may generally disclose multiplexing and demultiplexing between STM-0 signals and higher-order STM signals, Yamato does not disclose the features of claim 1 as suggested. Rather, as discussed below, Yamato discloses two signal paths through two separate communication devices. Each path will be considered below to illustrate that Yamato neither teaches nor suggests all of the features of the recited claim.

With respect to data flowing in a first direction, Yamato discloses a first communication device that receives a low-speed signal (STM-0), synchronizes it to a

reference clock, and supplies the result to a second communication device. For example, Yamato discloses:

> "The first communication device 2 receives data from the low-speed digital circuit, prepares serial data from the received data in synchronization with the reference clock signal, and sends the serial data and a frame signal to the second communication device 1." (Yamato, col. 7, lines 14-18).

Yamato further discloses the second communication device that receives low speed signals, multiplexes the received signals, and may then convert the resulting multiplexed signal into a high-speed signal for transmission onto a network. For example,

> "In the high-speed device 1, each electrical interface 15 receives a signal from the low-speed device 2 and multiplexes it into an STM (synchronous transfer module) signal. The high-speed multiplexer 12 simply multiplexes such STM signals from the electrical interfaces 15 into a multiplexed STM signal. An electrical-to-optical converter 16 converts the multiplexed STM signal into a multiplexed optical STM signal, e.g., an STM-16 signal of 2.4 Gb/s. " (Yamato, col. 8, lines 15-22).

Accordingly, Yamato merely discloses that the second communication device multiplexes low-speed signals into an STM signal. However, Applicant finds no teaching or suggestion of Yamato's first device, second device, or the combination of the two, as described above, recovering data from the tributary, converting the data recovered from the tributary into at least two low-speed data channels, and multiplexing the low-speed symbol channels to produce an electrical high-speed channel.

Turning next to data flowing in the reverse direction, as described below, Yamato discloses that the second communication device receives a high-speed signal from the network, demultiplexes it, and transmits the resulting signals via multiple electrical interfaces.

> "The high-speed device 1 receives a high-speed multiplexed optical STM signal, e.g., an STM-16 signal of 2.4 Gb/s. An optical-to-electrical converter 17 converts the optical signal into an electrical signal. The high-

> speed demultiplexer 14 demultiplexes the electrical signal into STM signals, which are transferred to the electrical interfaces 15. Each of the electrical interfaces 15 demultiplexes the received STM signal into a data signal for the first-order digital circuit or for the second-order digital circuit, or into a VC signal. The demultiplexed signal is transferred to the low-speed device 2. " (Yamato, col. 8, lines 23-34).

In addition, Yamato discloses that the first communication device receives serial data from the second communication device, prepares a data signal from it, and transmits the results as a low-speed signal (STM-0). For example, Yamato discloses:

> "The device 1 receives an STM signal from the STM circuit, prepares serial data from the STM signal in synchronization with the reference clock signal, and sends the serial data and a frame signal to the device 2. ... In the first communication device 2, a ... receiver 23 receives serial data from the device 1 and provides the terminator 21 with data to be transmitted to the low-speed digital circuit. ... The receiver 23 may provide the terminator 21 with serial data from the second communication device 1 as it is. Alternatively, the receiver 23 receives a VC signal from the device 1, decomposes the VC signal into a data signal, and provides the terminator 21 with the data signal." (Yamato, col. 7, lines 20-45).

Accordingly, Yamato's second communication device demultiplexes an STM-16 signal into multiple lower speed STM signals. The lower speed signals are received by the first communication device and provided to the low-speed digital circuit. Hence, again, Applicant finds no teaching or suggestion of "multiplexing the low-speed symbol channels" as recited. Further, it is noted that within the second communication device, the signals that are conveyed in the first direction discussed above are separate from the signals that are conveyed in the reverse direction. Applicant finds no teaching or suggestion of Yamato's first and second devices, either individually or in combination, "converting the recovered data into at least two low-speed data channels" and subsequently multiplexing data from the resulting channels either before or after modulating them to generate symbol channels, since Yamato's demultiplexing and multiplexing functions are operating upon separate data signals traveling in opposite directions. Accordingly, Applicant submits a prima facie case of obviousness has not been established and claim 1 is patentably distinguishable from the cited art for at least

the above reasons. As independent claim 21 includes limitations similar to those of claim 1, claim 21 is believed patentably distinguishable from the cited art for similar reasons. Likewise, each of dependent claims 2-11 and 22-29 are believed patentably distinguishable from the cited art for at least the above reasons as well.

In addition to the above, Applicant submits the dependent claims recite additional features which are neither taught nor suggested by the cited art. For example, Applicant submits that claim 8 recites limitations neither taught nor suggested by the cited art. In paragraph 12 of the present Office Action, the examiner states that Yamato in view of Shibagaki in further view of Doshi in further view of Applicant's admitted prior art discloses:

> "receiving the optical high-speed channel (Yamato, col. 8, lines 24-34); converting the received optical high-speed channel to a receive-side electrical high-speed channel (Yamato, col. 8, lines 24-34); frequency division demultiplexing the receive-side electrical high-speed channel into at least two receive-side low-speed symbol channels (Yamato, col. 8, lines 24-34 and Shibagaki: Fig. 2; col. 1, lines 39-42; and col. 4, lines 44-56); demodulating each receive-side low-speed symbol channel to generate a corresponding receive-side low-speed data channel (Shibagaki: Fig. 2; col. 1, lines 39-42; and col. 4, lines 44-56); recovering a clock and data from each receive-side low-speed data channel (Yamato, col. 2, lines 24-47 and col. 10, lines 33-40); generating a receive-side reference clock synchronized to the receive-side recovered data (Yamato, col. 2, lines 24-47; col. 7, lines 15-34; and col. 10, lines 33-40); and generating a receive-side tributary (low-speed signal), wherein the receive-side tributary contains all of the receive-side recovered data, and the receive-side tributary is timed by a clock based on the receive-side reference clock and complies with the jitter tolerance (Yamato, col. 4, lines 38-54; col. 5, lines 6-13; and col. 7, lines 15-34 and Applicant: page 3, lines 3-24, esp. page 3, lines 17-24).

However, claim 8 recites, in part:

"... receiving the optical high-speed channel;
converting the received optical high-speed channel to a receive-side electrical high-speed channel;

frequency division demultiplexing the receive-side electrical high-speed channel into at least two receive-side low-speed symbol channels;
demodulating each receive-side low-speed symbol channel to generate a corresponding receive-side low-speed data channel;
recovering a clock and **data from each receive-side low-speed data channel**;
generating a receive-side reference clock synchronized to the receive-side recovered data; **and**
generating a receive-side tributary, wherein the receive-side tributary contains all of the receive-side recovered data, and the receive-side tributary is timed by a clock based on the receive-side reference clock and complies with the jitter tolerance." (emphasis added).

It is noted that, as recited, data from the high-speed channel is demultiplexed into at least two low-speed channels that are subsequently used to generate a tributary that contains all of the receive-side recovered data. In contrast, Yamato merely discloses demultiplexing a high-speed signal into multiple low-speed signals and conveying a low-speed signal to a low-speed digital circuit. However, there is no disclosure that the multiple low-speed signals are used to generate a tributary that contains all of the data from the high-speed signal as recited.

As previously noted with regard to claim 1, Yamato discloses that in the reverse direction, the second communication device receives a high-speed signal from the network, demultiplexes it, and transmits each of the resulting signals to one of multiple electrical interfaces (15), which in turn dumultiplex the received signals. As disclosed by Yamato,

"The high-speed device 1 receives a high-speed multiplexed optical STM signal, e.g., an STM-16 signal of 2.4 Gb/s. An optical-to-electrical converter 17 converts the optical signal into an electrical signal. The high-speed demultiplexer 14 demultiplexes the electrical signal into STM signals, which are transferred to the electrical interfaces 15. Each of the electrical interfaces 15 demultiplexes the received STM signal into a data signal for the first-order digital circuit or for the second-order digital circuit, or into a VC signal. The demultiplexed signal is transferred to the low-speed device 2. " (Yamato, col. 8, lines 23-34).

It may be appreciated that demultiplexer 14 produces plural STM signals which are transferred to plural electrical interfaces 15, each of which interfaces to a low-speed

device 2. Applicant finds no teaching or suggestion in Yamato of generating a receive-side tributary, wherein the receive-side tributary contains all of the receive-side recovered data. Accordingly, Applicant submits that claim 8 is patentably distinguishable from the cited art for at least the above reasons. As independent claims 12 and 30 and dependent claim 27 include limitations similar to those of claim 8, claims 12, 27, and 30 are believed patentably distinguishable from the cited art for similar reasons. As each of dependent claims 9-11, 13-20, 28-29, and 31-36 includes the limitations of the independent claims and any intervening claims upon which it depends, each of dependent claims 9-11, 13-20, 28-29, and 31-36 is believed patentably distinguishable from the cited art for at least the above reasons.

Applicant believes all claims to be in condition for allowance. Should the examiner believe issues remain which would prevent the application from proceeding to allowance, the below signed representative request a telephone interview (512) 853-8866 in order to facilitate a speedy resolution.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5957-41406/RDR.

☒ Petition for Extension of Time

☒ Fee Authorization

☒ Return Postcard

Respectfully submitted,

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